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CLAIMS

What is claimed is:

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- using processor implementation-specific instructions to save a

 processor state in a system memory when a machine check

 error is generated by a processor;
- attempting to correct the error using processor implementationspecific instructions;
 - transferring control to processor-independent instructions; receiving control from processor-independent instructions; and returning to an interrupted context of the processor by restoring the processor state.
 - 2. The method of claim 1, further comprising providing processor error record information obtained using processor implementation—specific instructions.
- The method of claim 1, further comprising attempting to contain
 the error if a second processor is coupled to the processor by
 requesting a rendezvous between the processor and the second
 processor.
- 1 4. The method of claim 1, wherein receiving control from processor2 independent instructions indicates that the error has been
 3 corrected.

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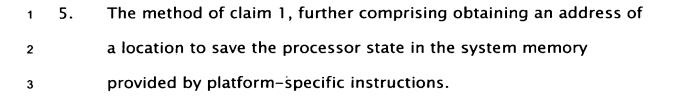
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- 1 6. The method of claim 1, wherein attempting to correct the error
 2 using processor implementation-specific instructions is not done if
 3 an expected machine check indicator is set.
 - 7. A machine-readable medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

using processor implementation-specific instructions to save the processor state in a system memory when a machine check error is generated by the processor;

attempting to correct the error using processor implementationspecific instructions;

transferring control to processor-independent instructions; receiving control from processor-independent instructions; and returning to an interrupted context of the processor by restoring the processor state.

1 8. The machine-readable medium of claim 7, wherein the operations
2 further comprise using processor implementation-specific
3 instructions to provide processor error record information
4 requested by processor-independent instructions.

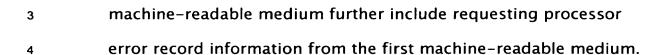
- 1 9. The machine-readable medium of claim 7, wherein the operations
 2 further comprise attempting to contain the error if a second
 3 processor is coupled to the processor by requesting a rendezvous
 4 between the processor and the second processor.
- 1 10. The machine-readable medium of claim 7, wherein receiving
 2 control from processor-independent instructions indicates that the
 3 error has been corrected.
 - 11. The machine-readable medium of claim 7, wherein the operations further comprise obtaining an address of a location to save the processor state in the system memory provided by platform-specific instructions.
- 1 12. The machine-readable medium of claim 7, wherein attempting to
 2 correct the error using processor implementation-specific
 3 instructions is not done if an expected machine check indicator is
 4 set.
- 1 13. The machine-readable medium of claim 7, wherein the instructions
 2 provided by the machine-readable medium are not cacheable by
 3 the processor.
- 1 14. A central processing unit (CPU) comprising:
- 2 a processor;

3	3	a first machine-readable medium coupled to the processor, the
4	1	first machine-readable medium including processor
. 5	5	implementation-specific instructions that, if executed by the
E	6	processor, will cause the processor to perform operations
7	7	including
8	3	saving the processor state in a system memory and
· (•	attempting to correct the error when a machine check
10)	error is generated by the processor, and
1 1 1	1	receiving control and returning to the interrupted context of
)] 12]	2	the processor by restoring the state of the processor
ີ] 13 ክ	3	when the error is determined to have been corrected;
] 14]	ı	a second machine-readable medium coupled to the processor, the
15	5	second machine-readable medium including only processor
16	5	implementation-independent instructions that, if executed by
17	,	the processor, will cause the processor to perform operations
18	3	including
19		receiving control from the first machine-readable medium;
20)	determining if the error has been corrected;
21		transferring control to the first machine-readable medium if
22	?	the error has been corrected.
1	15.	The central processing unit (CPU) of claim 14, wherein the

operations performed by the instructions provided by the second

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- 1 16. The central processing unit (CPU) of claim 14, wherein the
 2 operations performed by the instructions provided by the first
 3 machine-readable medium further include attempting to contain
 4 the error if a second processor is coupled to the processor by
 5 requesting a rendezvous between the processor and the second
 6 processor.
 - 17. The central processing unit (CPU) of claim 14, wherein the operations performed by the instructions provided by the second machine-readable medium further include providing an address of a location to save the processor state in the system memory to the first machine-readable medium.
- 1 18. The central processing unit (CPU) of claim 14, wherein attempting
 2 to correct the error is not done if an expected machine check
 3 indicator is set.
- 1 19. The central processing unit (CPU) of claim 14, wherein the
 instructions provided by the first and second machine-readable
 media are not cacheable by the processor.
- 1 20. The central processing unit (CPU) of claim 14, wherein the
 2 operations performed by the instructions provided by the second
 3 machine-readable medium further include if the error is

- 4 uncorrected, passing control to an operating system error handler if
- 5 present, otherwise, performing one of a halt and a reboot of the
- 6 CPU.